

Abstract

The invention is directed to improving power consumption in an integrated circuit by reducing the leakage current of a plurality of MOS transistors with an adaptive back biasing circuit. Since the leakage current characteristic is often non-linear, the optimal back bias voltage (lowest leakage current) is typically identifiable at an inflection point in a graph of the leakage current characteristic versus back bias voltage. Also, depending upon the doping of the MOS transistors (N versus P type) and manufacturing variables for a particular fabrication process, the position of this inflection point can vary between individual integrated circuits that implement substantially the same arrangement of MOS transistors. Despite these issues, the inventive circuit can substantially reduce the leakage current by coupling an adjusted back bias voltage to the substrate of an Integrated Circuit. The invention provides an adjusted back bias voltage to the bulk terminals (substrate) based on a determination of the inflection point for the leakage current characteristic in an individual integrated circuit.